A LEADING-EDGE HARDWARE FAMILY FOR LOW-LEVEL RF AND DIAGNOSTICS APPLICATIONS IN CERN'S SYNCHROTRONS

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M. E. Angoletta, A. Blas, M. Jaussi, P. Leinonen, T. Levens, J. Molendijk, J. Sanchez-Quesada, J. Simonin,
CERN, Geneva, Switzerland.

ABSTRACT

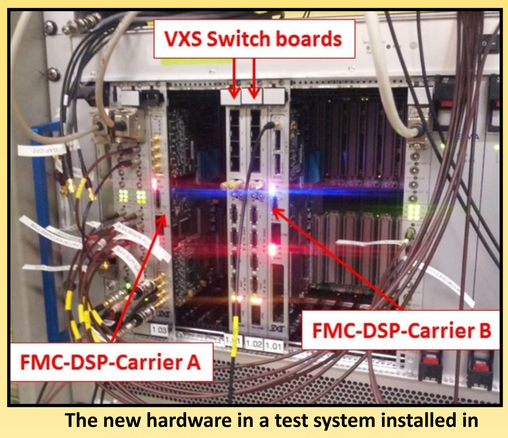
A leading-edge hardware family, evolution of that successfully deployed in CERN's Low-Energy Ion Ring (LEIR), is under development at CERN to address the LLRF needs of synchrotrons in the Meyrin site. It will be deployed in 2014 in the CERN's **PS Booster** and in the medical machine **MedAustron**. It will be then retro-fit to **LEIR** to standardise its LLRF implementation. It will also be used for the LLRF as well as longitudinal diagnostics implementation for the new Extra Low ENergy Antiproton (**ELENA**) Ring **(see poster #46)**, a new synchrotron that will be commissioned in 2016 to further decelerate the antiprotons transferred from the CERN's Antiproton Decelerator (AD).

The requirements for the LLRF as well as for the diagnostics systems are very demanding owing to the revolution frequency swing, dynamic range and low noise required by the cavity voltage control and digital signal processing to be performed.

OVERVIEW

The new hardware family [1] developed by CERN's RF Group, is an evolution of that successfully operational in CERN's LEIR since 2006 [2]. It will be deployed in the PSB [3] and MedAustron [4] in 2014, retrofit to LEIR in 2015 and deployed in ELENA [5] in 2016. Other synchrotrons will soon follow [6].

The family provides a very high processing power, is compact, flexible and modular.

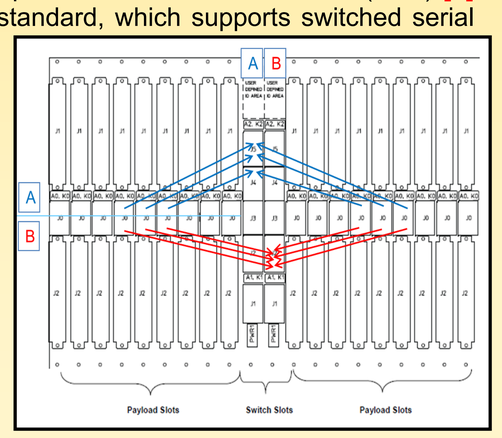


The new hardware in a test system installed in CERN's PSB during the 2012—2013 run

The hardware family is based upon the VME Switched Serial (VXS) [7] enhancement of the VME64x standard, which supports switched serial fabrics over a new, high-speed P0 connector.

The VITA57 standard FPGA Mezzanine Card (FMC) [8] is used for the daughtercards.

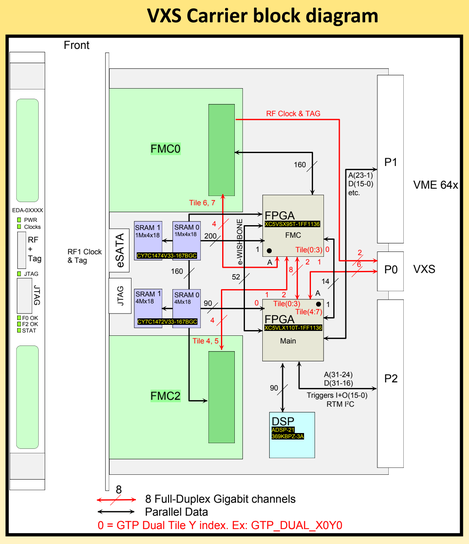
Many of the selected components, such as the motherboard's Virtex 5 FPGAs and the daughtercards' 16-bit ADCs and DACs, are amongst the most advanced units on the market.



VXS interconnect structure with two Switch boards

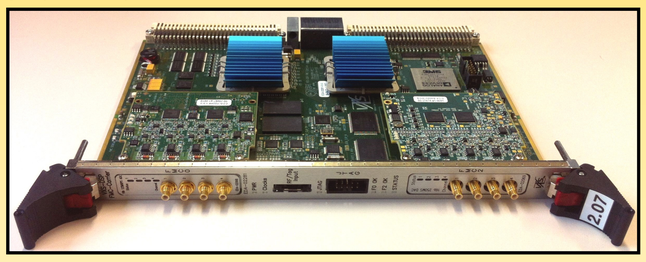
VXS CARRIER BOARD

VXS Carrier block diagram



The VXS-DSP-FMC Carrier board is a 6U unit board carrying:

- A SHARC Digital Signal Processor (DSP) ADSP-21368
- A Virtex 5 Field Programmable Gate Arrays (FPGAs) XC5VLX110T (**Main FPGA**)
- A Virtex 5 FPGA XC5VSX95T with DSP capabilities (**FMC FPGA**)
- Two dedicated full-duplex VXS channels from each Carrier board routing to Switch B distribute RF clock + TAG.
- Six full-duplex VXS channels, bonded to form three 32 bit data paths, to transfer 10b8b-encoded data between Carrier boards at a raw link rate of 2 Gbit/s or 100 MS/s (32 bit).



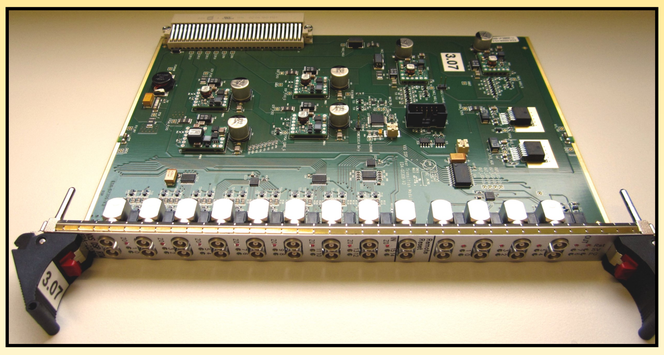
VXS Carrier with two daughtercards installed

The Carrier board can host up to two FMC daughtercards with a high-pin count format. It includes memory banks for observation purposes: two 4Mx18 bit banks clocked at 100 MS/s and two, 1Mx4x18 bit banks clocked at the RF clock frequency.

Several communication channels are implemented in the Main FPGA: **a)** VME64x (A32/D32); **b)** DSP (A16/D32); **c)** Carrier-to-Carrier (VXS full-duplex dual 32 bit link with a transfer rate of 100 MS/s); **d)** communication & data exchange with the FMC FPGA (full-duplex 32 bit Gigabit links); **e)** I^2C link to control the RTM configuration and LEDs; **f)** I^2C link to control the board front-panel LEDs; **g)** I^2C to control the VXS Switch module; **h)** I^2C links to exchange IPMI [9] information with the FMC FPGA. The communication architecture is configured such that no arbitration is required on any of the link nor bus interfaces for simplicity and overall system reliability.

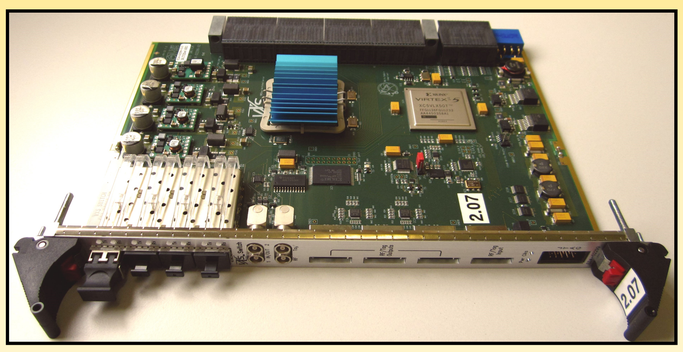
RTM MODULE

The RTM is the VXS-DSP-FMC Carrier companion board. Installed in the rear side of the VXS crate and interfaced to the Carrier via the J2/P2 connector, it carries all major secondary power supplies needed by the Carrier. The RTM front panel provides sixteen general purpose digital inputs and eight general-purpose digital outputs using stacked LEMO 00 connectors.



VXS SWITCH MODULE

The VXS Switch board allows using the VXS bus to interconnect boards via full-duplex Giga-bit serial links. Each VXS crate is fitted with two Switch boards each positioned at a starpoint, called "A" & "B" allowing to fully route a total of eight full-duplex up-to 3.125 Gbit/s from any payload slot to another. The Switch boards also implement a multi-cast capability used to distribute RF Clock + Tag across the VXS fabric.



CONCLUSIONS AND OUTLOOK

A leading-edge hardware family is under development at CERN to address the LLRF needs of synchrotrons in the Meyrin site. After being deployed in machines at CERN and abroad, it will be used for the LLRF and for the longitudinal diagnostics implementation in the ELENA ring.

This hardware family provides very high processing power by making advanced use of FPGA and DSP resources. Furthermore, it is compact, flexible and modular. Its planned wide-spread use will allow for an easier maintenance and a better spares management.

REFERENCES

[1] M. E. Angoletta et al., "***A Leading-Edge Hardware Family for Diagnostics Applications and Low-Level RF in CERN's ELENA Ring***", IBIC'13, Oxford, September 2013, TUPF28.

[2] M.E. Angoletta et al., "***CERN's LEIR Digital LLRF: System Overview and Operational Experience***", IPAC'10, Kyoto, May 2010, TUPEA057, p. 1464.

[3] M. E. Angoletta et al., "***CERN's PS Booster LLRF Renovation: Plans and Initial Beam Tests***", IPAC'10, Kyoto, May 2010, TUPEA056, p. 1461.

[4] http://www.medaustron.at/en/

[5] T. Eriksson (editor) et al., "***ELENA, an Updated Cost and Feasibility Study***", CERN-BE-2010-029.

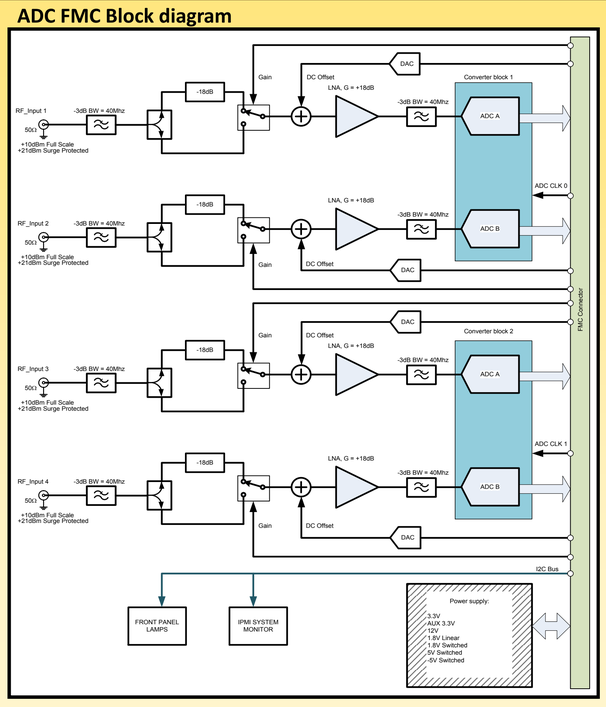
[6] T. Eriksson et al., "***Upgrades and Consolidation of the CERN AD for Operation During the Next Decades***", IPAC2013, Shanghai, China, May 2013, WEPEA063, p. 2654.

[7] http://www.vita.com/fmc.html

[8] http://www.vita.com/vxs.html

[9] Intel Hewlett-Packard NEC Dell, "***-IPMI- Intelligent Platform Management Interface Specification Second Generation***", June 2009.

ADC FMC Block diagram

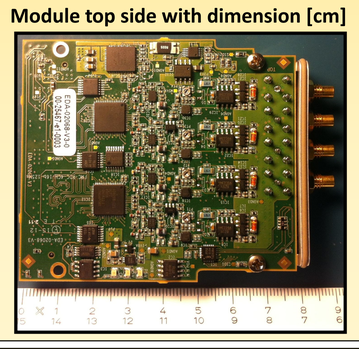


ADC MODULE

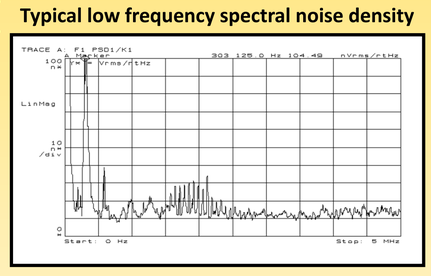
The ADC FMC daughtercard uses an AD9286 ADC and includes four independent digitisation channels with up to 125 MS/s and 16 bits. Its analogue front-end, based on the LT6409 IC, provides signal conditioning with DC coupling, low noise, low distortion and a controllable gain switching of 18 dB, corresponding to 3 LSBs.

- Measured wideband SFDR > 70 dB
- SNR > 74 dB
- ENOB = 12.5 bits (typical)
- Analogue BW = 300 MHz (max.)

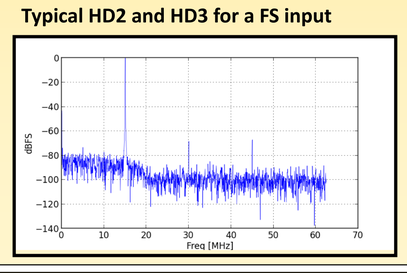
Module top side with dimension [cm]



Typical low frequency spectral noise density

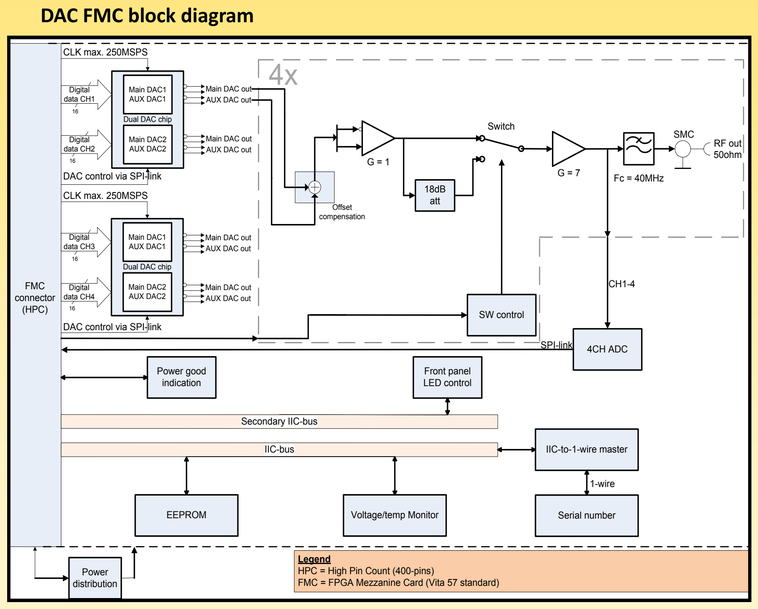


Typical HD2 and HD3 for a FS input



DAC MODULE

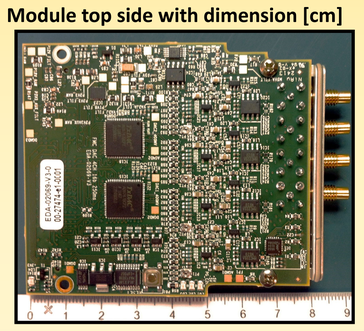
DAC FMC block diagram



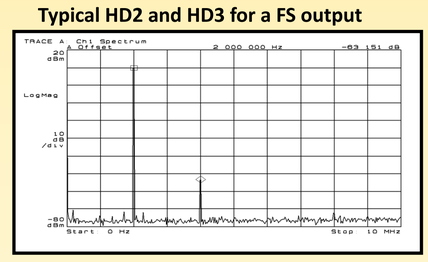
The DAC FMC daughtercard is based on the AD9747 DAC and allows four independent digital-to-analogue conversion channels with 16 bits resolution in the conversion and programmable gain switching of 18 dB. The output is DC coupled, with a 40 MHz analogue bandwidth and a full scale, peak output voltage of 3.6 V. The sampling rate of the DAC mezzanine can go up to 250 MS/s and the front-end, like the ADC board, includes low distortion and low noise electronics.

- Measured wideband SFDR: > 60 dB
- Gain switching settling time: < 30 nS

Module top side with dimension [cm]

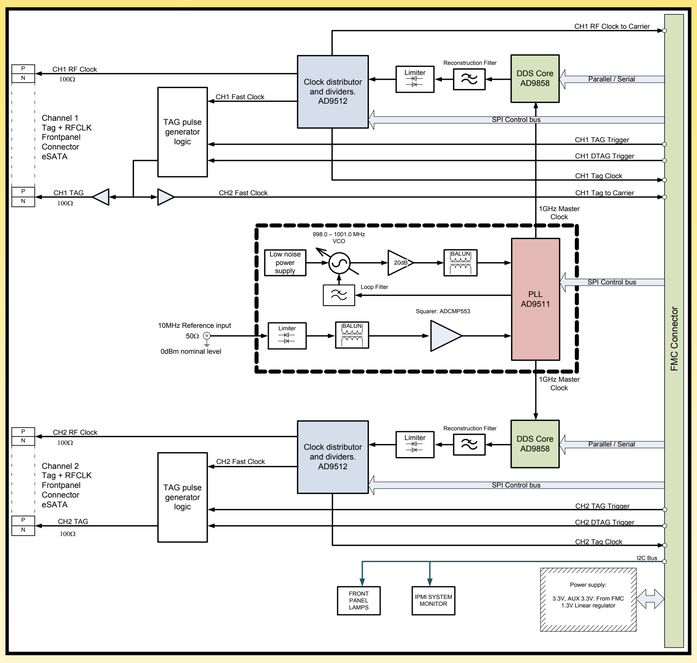


Typical HD2 and HD3 for a FS output



DDS MODULE

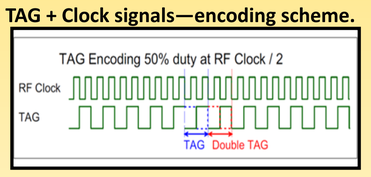
DDS FMC block diagram



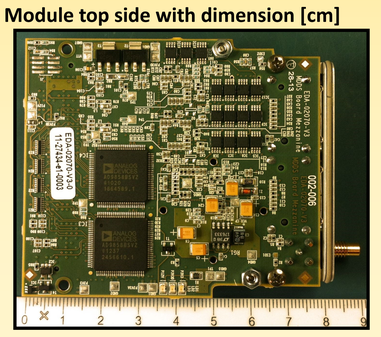
The DDS FMC daughtercard uses the AD9858 IC as the DDS core; it is a high quality, compact clock generator, featuring two independent channels synchronised to the same reference and allowing up to 232 mHz frequency step resolution.

- Typical jitter figure: ~800 fS (max. 2 pS for certain DDS output frequencies).
- Output divider combinations: 1:1 to 1:32
- Frequency resolution: 32 bits
- Generates the TAG signal to synchronize all DDC & SDDS channels.

TAG + Clock signals—encoding scheme.



Module top side with dimension [cm]



Typical phase noise plot for a 125MHz output.